WHAT IS CLAIMED IS:

1. A receive block for asynchronous transfer mode (ATM) cell delineation, comprising:

a plurality of cell delineation blocks each coupled to receive an associated serial bit stream, each cell delineation block operating to identify ATM cell boundaries in the serial bit stream and convert ATM cell payloads to parallel data words;

a memory having a plurality of memory blocks organized having a memory block associated with each cell delineation block, each memory block having a plurality of ATM cell storage locations;

a memory controller coupled to the cell delineation blocks and the memory, the memory controller operating to read data words from the cell delineation blocks and write data words to one of the cell storage locations in associated memory blocks; and

a bus controller coupled to the memory controller and to the memory, the bus controller operating to interface with an ATM physical layer, to receive a memory status signal from the memory controller and to provide signals to the memory for communicating an ATM cell across the ATM physical layer.

2. The receive block of Claim 1, wherein the bus controller further receives address mode/select signals and operates to respond to one of a plurality of subsets of port addresses on the ATM physical layer responsive to the address mode/select signals.

3. The receive block of Claim 3, wherein the plurality of subsets include four subsets.

4. The receive block of Claim 1, wherein the plurality of cell delineation blocks includes eight cell delineation blocks.

5. The receive block of Claim 4, wherein the plurality of memory blocks includes eight memory blocks each with two ATM cell storage locations.

6. The receive block of Claim 1, wherein each cell delineation block comprises:

a cell delineation unit receiving the serial bit stream, the cell delineation unit identifying ATM cell boundaries and providing an output serial bit stream of ATM cell payload;

a descrambler receiving the output serial bit stream of ATM cell payload, the descrambler operating to descramble the bit stream; and

a serial/parallel converter receiving the descrambled bit stream, the serial/parallel converter operating to convert the bit stream to parallel data words.

7. The receive block of Claim 1, wherein the ATM physical layer is a Utopia 2 interface.

8. A transmit block for asynchronous transfer mode (ATM) cell delineation, comprising:

a bus controller operating to interface with an ATM physical layer and to receive ATM cells across the ATM physical layer, the bus controller further operating to convert ATM cell payloads to output parallel data words;

a plurality of queue memories each having a plurality of cell storage locations;

a plurality of queue select devices coupled to the bus controller and receiving the output parallel data words, each queue select device providing the output parallel data words to one of the plurality of cell storage locations in an associated queue memory; and

a plurality of cell delineation blocks each receiving parallel data words from an associated queue memory, each cell delineation block operating to convert parallel data words to a serial bit stream carrying ATM cell payloads.

9. The transmit block of Claim 8, wherein the bus controller further receives address mode/select signals and operates to respond to one of a plurality of subsets of port addresses on the ATM physical layer responsive to the address mode/select signals.

10. The transmit block of Claim 9, wherein the plurality of subsets include four subsets.

11. The transmit block of Claim 8, wherein the plurality of cell delineation blocks includes eight cell delineation blocks.

12. The transmit block of Claim 11, wherein the plurality of queue memories includes eight queue memories each with two ATM cell storage locations.

13. The transmit block of Claim 8, wherein each cell delineation block comprises:

a multiplexer receiving parallel data words from each of the plurality of ATM cell storage locations in the associated queue memory, the multiplexer selecting on of the parallel data words and providing it as an output;

a parallel/serial converter receiving the output of the multiplexor and operating to convert the parallel data word to a serial bit stream; and

a descrambler receiving the serial bit stream and operating to scramble the bit stream and provide the scrambled bit stream as an output.

14. The transmit block of Claim 8, wherein the ATM physical layer is a Utopia 2 interface.